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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,274	06/27/2003	Satoshi Seo	60188-566	4710

7590 04/19/2005

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/607,274	SEO ET AL.
	Examiner	Art Unit
	Khiem D. Nguyen	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 31st, 2005 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-7 and 11-14) are pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

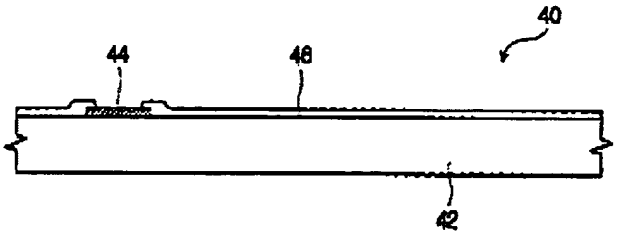
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang (U.S. Pub. 2002/0020855) in view of the applicant's admitted prior art (AAPA) of this application.

In re claim 1, **Hwang** discloses a method for fabricating a semiconductor device, the method comprising the steps of:

(a) forming bonding pads **44** above a wafer **42** on which semiconductor elements (Integrated circuits, not shown) and an interconnect layer (not shown) are formed (page 2, paragraph [0026] and FIG. 5);

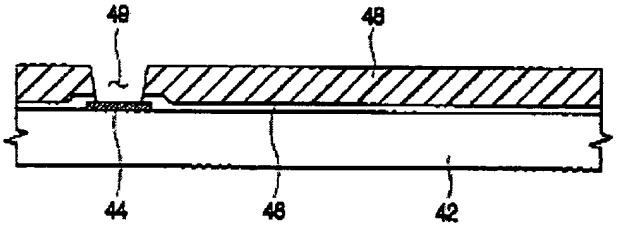
FIG. 5



(b) forming a passivation film **46** having apertures (at portion **49**) including regions of the passivation film located above parts of the bonding pads after the step (a) (page 2, paragraph [0026] and FIG. 5);

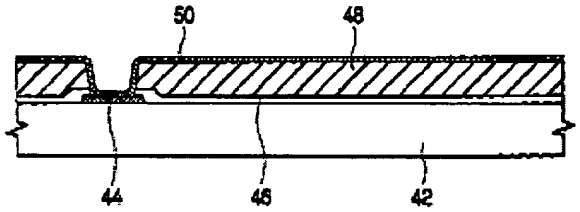
(c) forming a buffer coat film **48** for covering part of the passivation film **46** after the step (b) (page 2, paragraph [0027] and FIG. 6);

FIG. 6



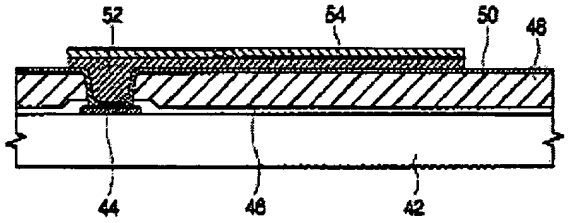
(d) forming, in the buffer coat film **48**, apertures (at portion **49**) including regions of the buffer coat film located on the whole periphery region having a certain distance from the periphery of the wafer, above scribe line regions and above the parts of the bonding pads, respectively (page 2, paragraphs [0028]-[0029] and FIGS. 6-7); and

FIG. 7



(e) bonding a surface protection tape **54** to the wafer **42** using an adhesive material **50** after the step (d) (page 2, paragraph [0030] and FIG. 9);

FIG. 9

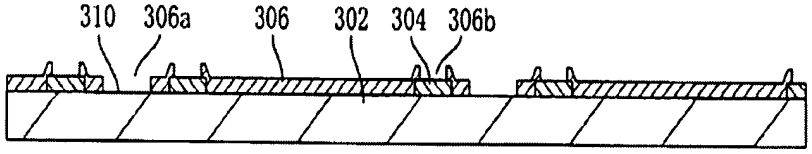


Hwang does not explicitly disclose polishing the rear surface of the wafer after the step (e) as recited in the Applicants' claimed invention.

AAPA, however, discloses a method for fabricating a semiconductor device, the method comprising the steps of (Background of the invention, pages 1-2 and FIGS. 20A-22):

(a) forming bonding pads **304** above a wafer **302** on which semiconductor elements (not shown) and an interconnect layer (not shown) are formed (page 1, lines 10-16 and FIG. 20A);

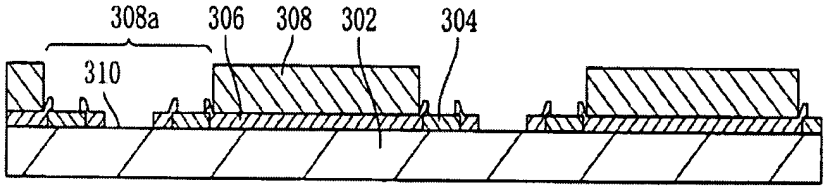
FIG. 20A



(b) forming a passivation film **306** having apertures **306a and 306b** including regions of the passivation film located above parts of the bonding pads after the step (a) (page 1, lines 16-21 and FIG. 20A);

(c) forming a buffer coat film **308** for covering part of the passivation film after the step (b) (FIG. 20B);

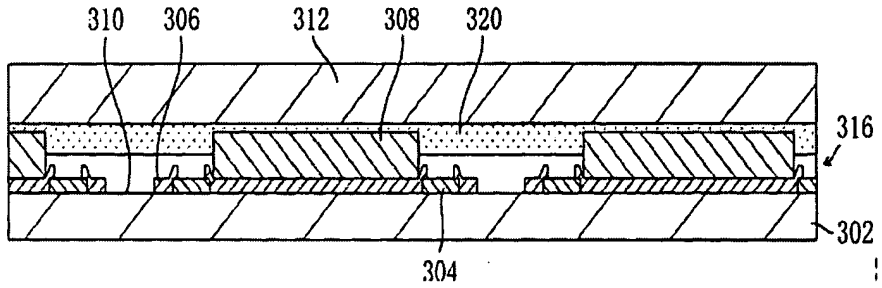
FIG. 20B



(d) forming, in the buffer coat film, apertures **308a** including regions of the buffer coat film located above scribe line regions and above the parts of the bonding pads, respectively (page 1, line 22 to page 2, line 5 and FIG. 20B);

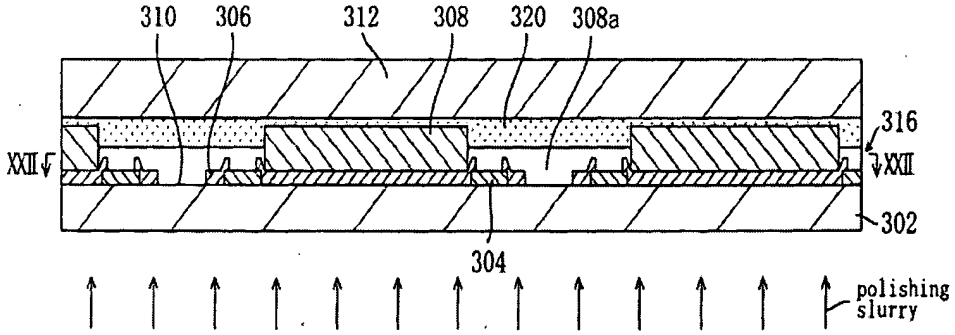
(e) bonding a surface protection tape **312** to the wafer using an adhesive material **320** after the step (d) (page 2, lines 2-5 and FIG. 21A); and

FIG. 21A



(f) polishing the rear surface of the wafer after the step (e) **(polishing slurry)** (page 2, lines 6-14 and FIG. 21B).

FIG. 21B

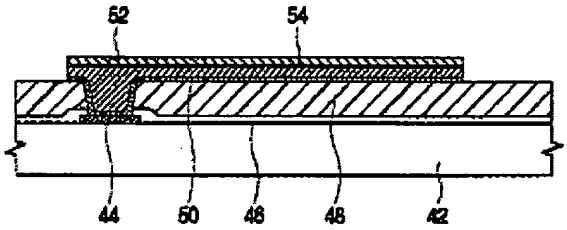


Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Hwang and AAPA to enable the process of polishing the rear surface of the wafer after the step (e) of Hwang to be performed so that the generated swarf is eliminated together with the polishing slurry (page 2, lines 6-10, AAPA).

In re claim 2, **Hwang** discloses that in the step (c), the buffer coat film 48 is formed using a positive-type photosensitive material (page 2, paragraph [0027]), and the step (d) includes a process for exposing part of the buffer coat film **48** located on the periphery region of the wafer (FIG. 10). Alternatively, AAPA also disclose that the

buffer coat film is formed using a positive-type photosensitive material (page 1, lines 22-24).

FIG. 10



In re claim 3, **Hwang** discloses that in the step (c), the buffer coat film **48** is formed using a positive-type photosensitive material (page 2, paragraph [0027]), and the step (d) includes a process for exposing part of the buffer coat film 48 located on the wholes of chip regions at least partly overlapped with the periphery region of the wafer (FIG. 10).

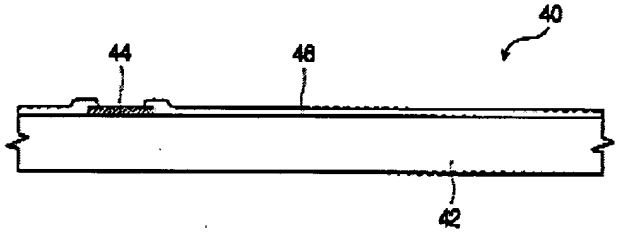
In re claim 4, **Hwang** and **AAPA** disclose that in the step (c), the buffer coat film 48 is formed using an organic resin (page 2, paragraph [0027]), and the step (d) includes a process for selectively removing part of the buffer coat film located on the periphery region of the wafer by a solvent (AAPA, page 1, lines 22-24).

In re claim 5, **Hwang** discloses that in the step (c), the buffer coat film **48** is formed using an organic resin (page 2, paragraph [0027]), and the step (d) includes a process for blowing gas on part of the buffer coat film located on the periphery region of the wafer before the curing (300°C for about 2 hours) of the buffer coat film (page 2, paragraph [0027]).

In re claim 6, **Hwang** discloses a method for fabricating a semiconductor device, the method comprising the steps of:

(a) forming bonding pads **44** above a wafer **42** on which semiconductor elements (Integrated circuits, not shown) and an interconnect layer (not shown) are formed (page 2, paragraph [0026] and FIG. 5);

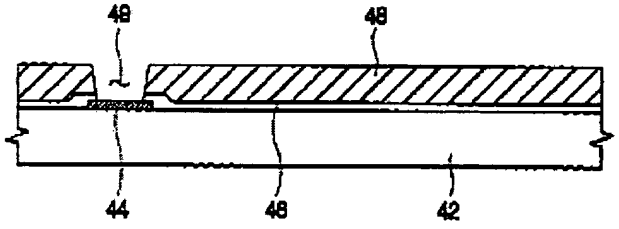
FIG. 5



(b) forming a passivation film **46** having apertures (at portion **49**) including regions of the passivation film located above parts of the bonding pads after the step (a) (page 2, paragraph [0026] and FIG. 5);

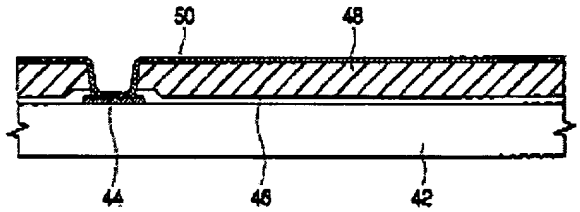
(c) forming a buffer coat film **48** for covering part of the passivation film **46** after the step (b) (page 2, paragraph [0027] and FIG. 6);

FIG. 6



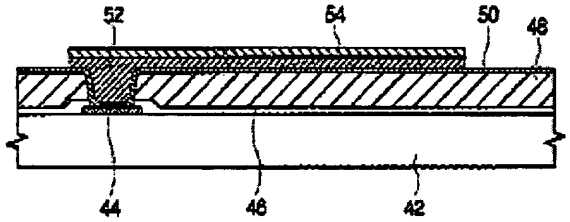
(d) forming, in the buffer coat film **48**, apertures (at portion **49**) including regions of the buffer coat film located above scribe regions and above parts of the bonding pads, respectively, and reducing the thickness of part of the buffer coat film located on the whole periphery region of the wafer having a certain distance from the periphery of the wafer (page 2, paragraphs [0028]-[0029] and FIGS. 6-7); and

FIG. 7



(e) bonding a surface protection tape **54** to the wafer **42** using an adhesive material **50** after the step (d) (page 2, paragraph [0030] and FIG. 9);

FIG. 9

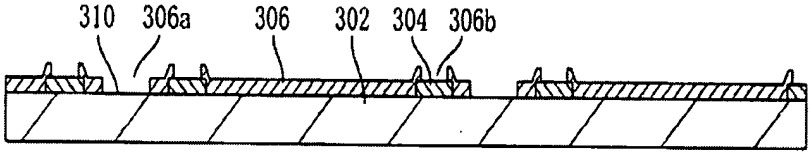


Hwang does not explicitly disclose polishing the rear surface of the wafer after the step (e) as recited in the Applicants' claimed invention.

AAPA, however, discloses a method for fabricating a semiconductor device, the method comprising the steps of (Background of the invention, pages 1-2 and FIGS. 20A-

22): (a) forming bonding pads **304** above a wafer **302** on which semiconductor elements (not shown) and an interconnect layer (not shown) are formed (page 1, lines 10-16 and FIG. 20A);

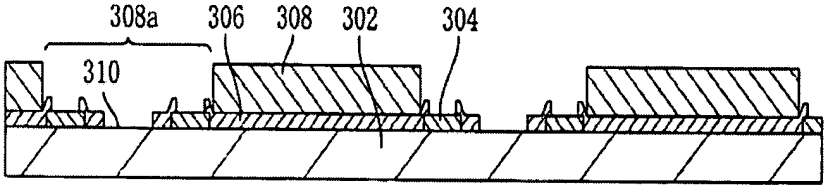
FIG. 20A



(b) forming a passivation film **306** having apertures **306a and 306b** including regions of the passivation film located above parts of the bonding pads after the step (a) (page 1, lines 16-21 and FIG. 20A);

(c) forming a buffer coat film **308** for covering part of the passivation film after the step (b) (FIG. 20B);

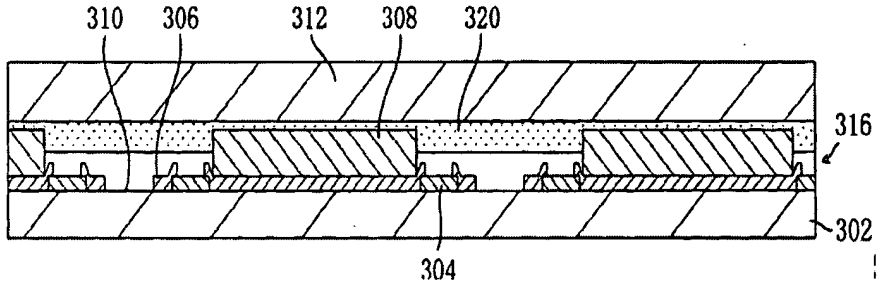
FIG. 20B



(d) forming, in the buffer coat film, apertures **308a** including regions of the buffer coat film located above scribe line regions and above the parts of the bonding pads, respectively (page 1, line 22 to page 2, line 5 and FIG. 20B);

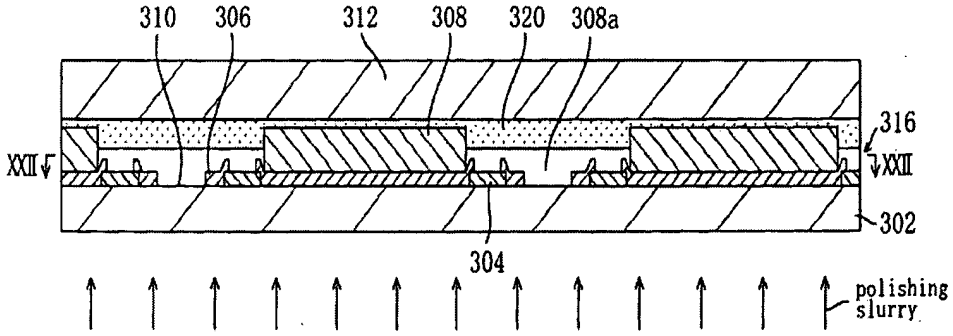
(e) bonding a surface protection tape **312** to the wafer using an adhesive material **320** after the step (d) (page 2, lines 2-5 and FIG. 21A); and

FIG. 21A



(f) polishing the rear surface of the wafer after the step (e) **(polishing slurry)** (page 2, lines 6-14 and FIG. 21B).

FIG. 21B

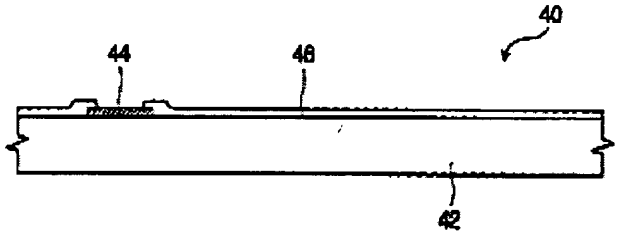


In re claim 7, **Hwang** discloses that in the step (d), the thickness of part of the buffer coat film located on the periphery region is reduced to 3μm or less (page 2, paragraph [0027]).

In re claim 11, **Hwang** discloses a method for fabricating a semiconductor device, the method comprising the steps of:

(a) forming bonding pads **44** above a wafer **42** on which semiconductor elements (Integrated circuits, not shown) and an interconnect layer (not shown) are formed (page 2, paragraph [0026] and FIG. 5);

FIG. 5



(b) forming a passivation film **46** having apertures (at portion 49) including regions of the passivation film located above parts of the bonding pads after the step (a) (page 2, paragraph [0026] and FIG. 5);

(c) forming a buffer coat film **48** for covering part of the passivation film 46 after the step (b) (page 2, paragraph [0027] and FIGS. 6-7);

FIG. 6

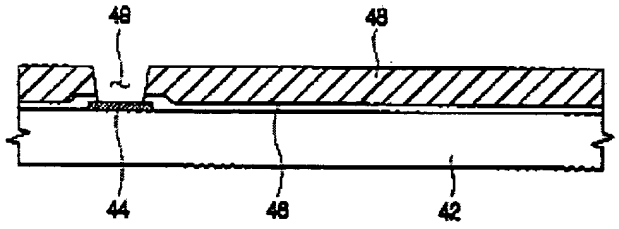
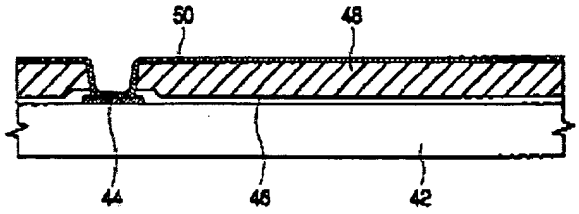


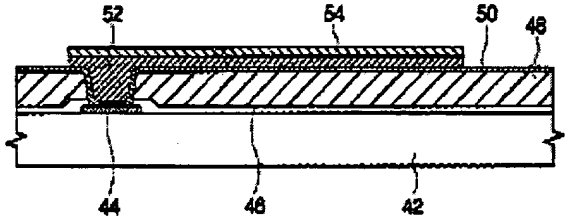
FIG. 7



(d) forming, in the buffer coat film **48**, apertures (at portion **49**) including regions of the buffer coat film located above part of scribe line regions and above parts of the bonding pads with connection parts connecting the adjacent chip regions formed by connecting four corners of each chip left among the apertures (page 2, paragraphs [0028]-[0029]); and

(e) bonding a surface protection tape **54** to the wafer **42** using an adhesive material **50** after the step (d) (page 2, paragraph [0030] and FIG. 9);

FIG. 9

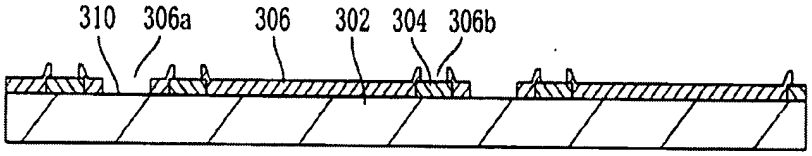


Hwang does not explicitly disclose polishing the rear surface of the wafer after the step (e) as recited in the Applicants' claimed invention.

AAPA, however, discloses a method for fabricating a semiconductor device, the method comprising the steps of (Background of the invention, pages 1-2 and FIGS. 20A-

22): (a) forming bonding pads **304** above a wafer **302** on which semiconductor elements (not shown) and an interconnect layer (not shown) are formed (page 1, lines 10-16 and FIG. 20A);

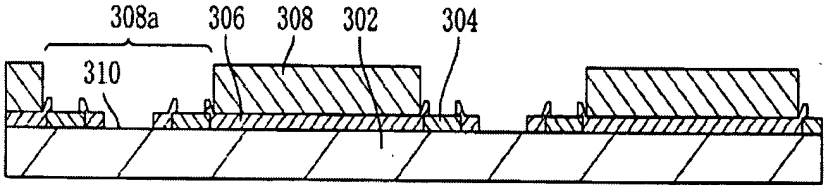
FIG. 20A



(b) forming a passivation film **306** having apertures **306a and 306b** including regions of the passivation film located above parts of the bonding pads after the step (a) (page 1, lines 16-21 and FIG. 20A);

(c) forming a buffer coat film **308** for covering part of the passivation film after the step (b) (FIG. 20B);

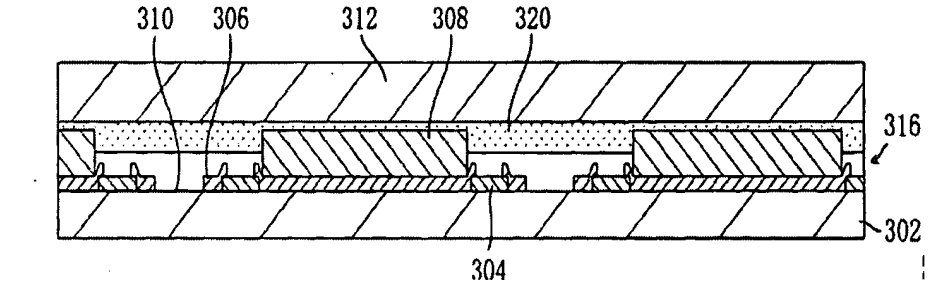
FIG. 20B



(d) forming, in the buffer coat film, apertures **308a** including regions of the buffer coat film located above scribe line regions and above the parts of the bonding pads, respectively (page 1, line 22 to page 2, line 5 and FIG. 20B);

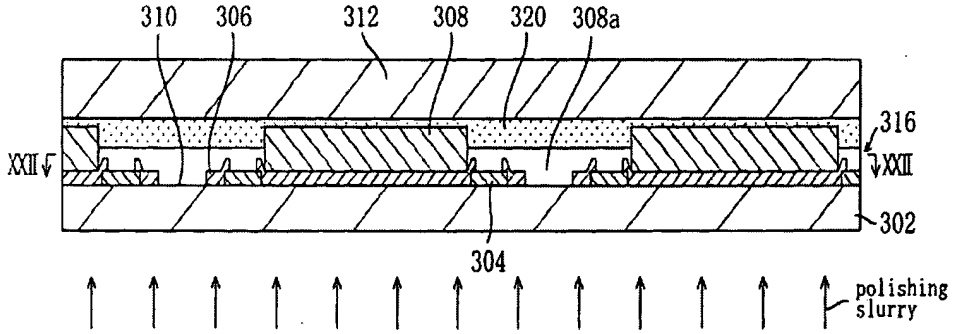
(e) bonding a surface protection tape **312** to the wafer using an adhesive material **320** after the step (d) (page 2, lines 2-5 and FIG. 21A); and

FIG. 21A



(f) polishing the rear surface of the wafer after the step (e) **(polishing slurry)** (page 2, lines 6-14 and FIG. 21B).

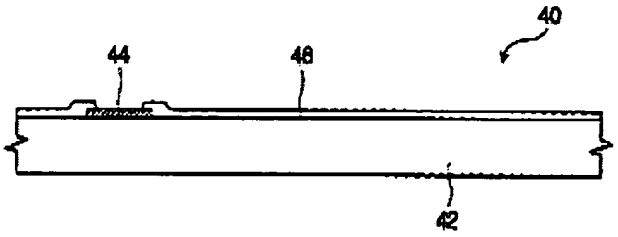
FIG. 21B



In re claim 12, **Hwang** discloses a semiconductor device comprising:

a semiconductor substrate **42** on which semiconductor elements (Integrated circuits, not shown) and an interconnect layer (not shown) are formed (page 2, paragraph [0026] and FIG. 5);

FIG. 5



bonding pads **44** formed above the semiconductor substrate (page 2, paragraph [0026] and FIG. 5);

a passivation film **46** formed above the semiconductor substrate and having apertures at which parts of the bonding pads are exposed (page 2, paragraph [0026]); and

a buffer coat film **48** that covers part of the passivation film **46** (page 2, paragraph [0027] and FIGS. 6-7) and has apertures (at portion **49**) obtained by removing reiongs of the buffer coat film located above parts of scribe line regions and above parts of the bonding pads with connection parts connecting the adjacent chip regions formed by connecting four corners of each chip left among the apertures (page 2, paragraphs [0028]-[0029]).

FIG. 6

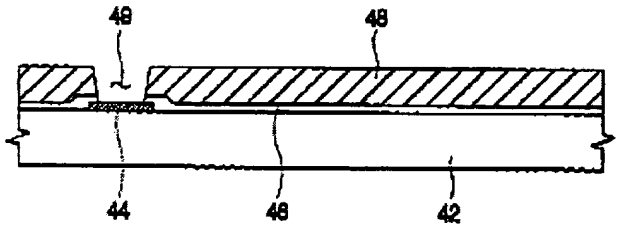
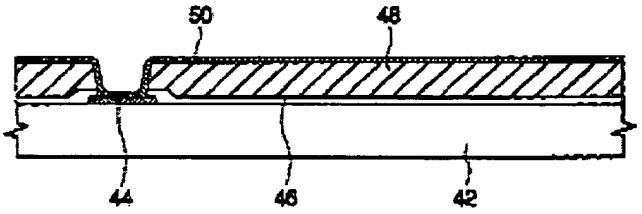


FIG. 7



In re claims 13 and 14, **Hwang** disclose that in the step (d) the whole periphery region refers to circular regions in the periphery of the wafer **42** (page 2, paragraphs [0028]-[0029]).

Response to Applicant's Amendment and Arguments

Applicants contend that neither AAPA nor Wakabayashi (U.S. Patent 6,607,970), alone or in combination, disclose or suggest forming, in the buffer coat film, apertures including regions of the buffer coat film located on the whole periphery region having a certain distance from the periphery of the wafer, above scribe line regions and above the parts of the bonding pads, respectively".

In response to Applicants' contention that neither AAPA nor Wakabayashi, alone or in combination, disclose or suggest forming, in the buffer coat film, apertures including regions of the buffer coat film located on the whole periphery region having a certain distance from the periphery of the wafer, above scribe line regions and above the parts of the bonding pads, respectively", Examiner respectfully disagrees. Applicants' argument is moot since the newly discovered reference, Hwang (U.S. Pub. 2002/0020855) in combination with AAPA disclose the Applicants' currently amended

claimed invention (Applicants are directed to, page 2, 2nd paragraph to page 6, 2nd paragraph of the 35 U.S.C. 103(a) rejection presented in this Office Action).

For these reasons, examiner holds the rejection proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
April 14th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER